IN THE SPECIFICATION:

Please amend the specification pursuant to 37 C.F.R. §1.121 as follows (see the accompanying "marked up" version pursuant to 1.121):

On page 6, delete the second paragraph and insert the following new second paragraph:

Each register access path 12, 14 carries three addresses from the accessing unit, two source addresses SRC1, SRC2 and a destination address DST. In the case of data processing operations, the source addresses SRC1, SRC2 define registers in the register files 10,11 which hold source operands for processing by the data processing unit. The destination address DST identifies a destination register into which a result of data processing will be placed. The operands and results are conveyed between the register file 10 or 11 and the respective data processing unit via the access paths 12, 14. In the case of load/store operations, the instruction formats allow memory access addresses A_x, A_y to be formulated from data values held in the registers as described in our copending application (GB-9916564.9, entitled An Instruction Set for a Computer), co-pending U.S. Application Serial No. 09/395,295. The load/store units access a common address space in the form of a data memory 16 via a dual ported data cache DCACHE 15. For this purpose, each load/store unit has a 64 bit data bus Dx,Dy and a 64 bit address bus Ax,Ay.

On page 10, delete the second paragraph and insert the following new second paragraph:

When the decode unit detects the combination denoting a long instruction at bits 29 to 31 and bit 63, the machine operates differently depending on the nature of the instruction. For register/register instruction format L2, the single opcode portion of the 64 bit word is duplicated into the X and Y-channels

along path 5_x,5_y to instruct the relevant data processing units in each of the X and Y channels simultaneously to perform the same operation. However, the registers are differently identified, each of the X and Y-channels receiving information identifying their particular registers such that the functional unit in the X channel accesses its registers (Src1, Src2, Dest1) and the functional unit in the Y channel accesses its registers (Src3, Src4, Dest2). Thus, format L2 in Figure 5 allows register to register data processing. For format L3 which allows for register/immediate data processing operations, a 64 bit word identifies a destination register Dest1 and a source register Src1 and defines a 32 bit immediate value. In high and low portions. For the adib/h/w instructions, the immediate value is duplicated to make a 64 bit value which can be added to the 64 bit contents of the source register Src1 and the results loaded into the destination register Dest1.

IN THE CLAIMS:

Please amend the claims pursuant to 37 C.F.R. §1.121 as follows (see the accompanying "marked-up" version pursuant to 1.121):

3. (Amended) A computer system according to claim 1, wherein when the decode unit detects that the instruction defines a single operation, it controls the first and second channels each to cooperate to simultaneously execute said single operation.